REMARKS

Claims 1 - 4 are presently pending in the application.

I. Claim Objections

Claims 1 and 3 stand objected to for informalities. These informalities are corrected as shown in the above Listing of Claims. Accordingly, the Examiner is respectfully requested to withdraw this objection.

II. Rejection of Claims 3 and 4 Under 35 U.S.C. § 102

Claims 3 and 4 stand rejected under 35 U.S.C. § 102 as allegedly being anticipated by U.S.P. No. 5,602,509 ("Kimura"). This rejection is respectfully traversed as explained below.

Independent claim 3 recites (among other things) a current source coupled between ground and the commonly coupled source electrodes (as shown in Figs. 1 - 3 and 6 - 17). At least these features are absolutely absent in the prior art cited as the basis for rejection. Accordingly, the instant § 102 rejection cannot stand because a "claim is anticipated only if each and every element as set forth in the claim is found . . . in a single prior art reference." *See* M.P.E.P. § 2131.

To explain in greater detail, the instant rejection compares Figure 3 of the Kimura reference to the above-noted features of independent claim 3. However, nowhere in the Kimura reference can the above-noted features of independent claim 3 be found. Indeed, the Kimura reference discloses something entirely different than the above-noted features of independent claim 3. That is, Figure 3 of the Kimura reference shows a constant current source aI coupled

between the commonly coupled source electrodes of a differential pair of transistors and a negative supply voltage, V^- (*see* also Col. 2, lines 66 - 67).

Accordingly, independent claim 3 is patentable at least because the claim recites features that are absolutely undisclosed and unsuggested by the prior art used as the basis for rejection. In light of the above-noted deficiencies of the prior art used to reject claim 3, it is asserted that this claim is patentable and the Examiner is therefore respectfully requested to reconsider and withdraw the instant rejection. As to claim 4, this claim is asserted as patentable at least by virtue of its dependency upon independent claim 3.

Additionally as to the 35 U.S.C. § 102 rejection of claims 3 and 4, it is further asserted that the circuit shown in Figure 3 of the Kimura reference fails to include an output terminal for outputting a voltage to be added. Furthermore, most electronic circuits of modern creation are realized as integrated circuits. Hence, even if a circuit were to create a voltage to be added, without an output terminal it is impossible to utilize that signal because there fails to be an output lead wire to transfer the signal. Along these same lines, it is impossible to utilize any addition signal if a person does not know that the circuit has a node from which an addition output signal is obtained.

With further respect to claim 4, this claim is rejected under 35 U.S.C. § 102 in view of Figure 1 of the Kimura reference. As to the circuit shown in Figure 1 of the Kimura reference, transistor M55 is not driven by a constant current. Rather M55 functions as a current bypass element through which a current obtained by subtracting drains the currents of transistors M51 and M52 from the constant current of aI as it flows from node A to node B. Therefore, the

transistor M55 differs from a commonly known level shifter which performs level-shifting by a constant voltage. If the drains of the transistors M51 and M52 are not coupled to the drain of transistor M55, the circuit including transistor M55 forms a commonly known level shifter. However, in practice, the MOSFET M55 and the current sink disposed near the node A serve as a current level shifter for shifting the current level at node A to that current level present at node B (as described at Col. 2, lines 51 - 55 of the Kimura reference). Therefore, the Kimura reference does not teach "a level shifter for level-shifting the voltage[,]" as such is recited by claim 4. Accordingly, claim 4 is further asserted as patentable at least for these additional reasons.

III. Rejection of Claims 1 and 2 Under 35 U.S.C. § 103

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as allegedly obvious in view of U.S.P. No. 5,602,509 ("Kimura"). For the following reasons, this rejection is respectfully traversed.

Independent claim 1 includes features that are similar in nature to those features explained above in Part II of this Paper (*i.e.*, a current source coupled between ground and the commonly coupled source electrodes). These features are absolutely absent in the prior art used as the basis for rejection. Accordingly, because prima facie obviousness requires that "all of the claim limitations must be taught or suggested by the prior art[,]" (*see* M.P.E.P. § 2143.03) and further because the prior art is absolutely deficient in teaching all of the features of independent claim 1, independent claim 1 is therefore patentable. The Examiner is therefore respectfully requested to reconsider and withdraw this rejection.

Furthermore, claim 2 is asserted as patentable at least by virtue of its dependency upon claim 1 and further because the Kimura reference fails to teach or suggest "a level shifter for level-shifting the voltage[,]" as such is recited by claim 2 (and as explained above in Part II of this Paper).

With further respect to independent claim 1, it is additionally asserted that the inventor of the Kimura reference (Dr. Kimura, who is also the inventor of the instant application) was not aware that an addition voltage is obtained from the circuit of Figure 3 at the time the inventor invented the circuit. Accordingly, it is respectfully asserted that it is therefore impossible for those of ordinary skill in the art to realize a circuit that operates simultaneously as a voltage adder circuit and a voltage subtractor circuit, as is recited by independent claim 1. Independent claim 1 is therefore asserted as patentable at least for these additional reasons.

III. Conclusion

Because the instant invention recites features that are absolutely absent from the prior art used as the basis for rejection (as explained above), it is respectfully asserted that the instant rejections cannot stand. Accordingly, it is respectfully requested that the Examiner reconsider and withdraw this instant rejections.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Jason C. Beckstead
Registration No. 48,232

SUGHRUE MION, PLLC
Telephone: (650) 625-8100
Facsimile: (650) 625-8110

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: February 6, 2004